Jack Melcher

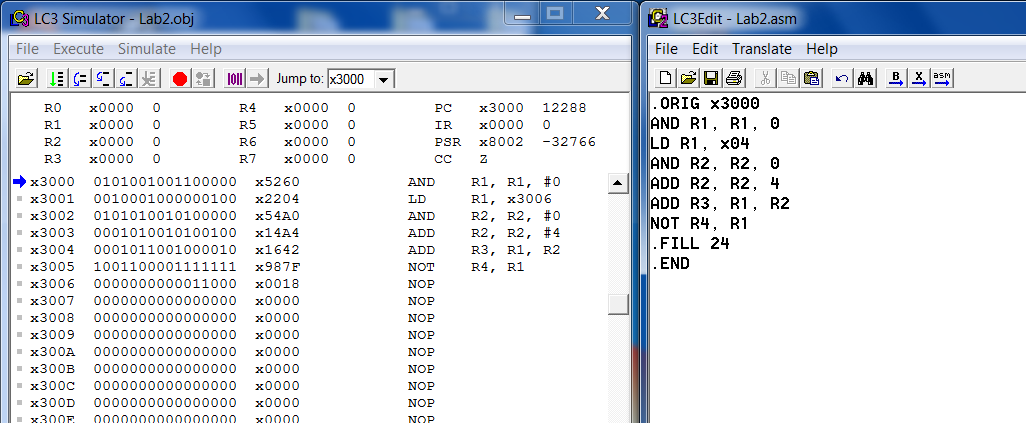
SID: 67574625

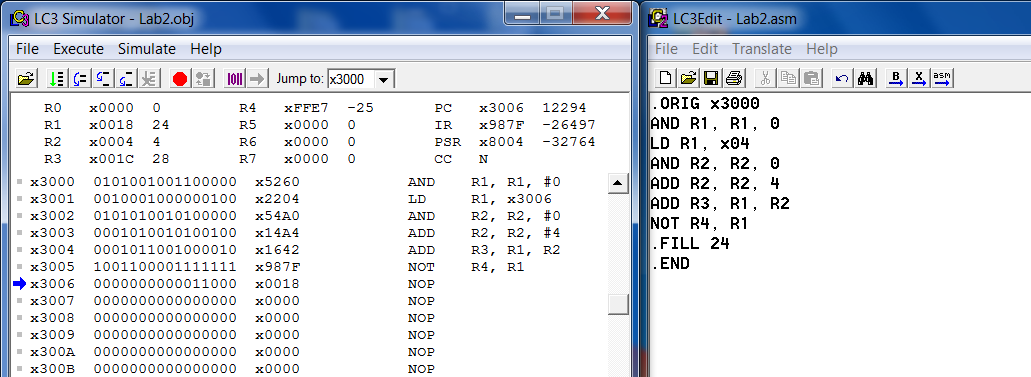
EECS 20

Lab 2

**Part A**

Use LC-3 simulator, write and run a program in an assembly language. This program loads R1, and R2 registers with numbers 24 and 4 respectively and save the sum of these two numbers in the register R3, and the complement (NOT) of R1 into register R4.





**Part B**

Find **Opcode** in decimal for the following instructions:

|  |  |  |
| --- | --- | --- |
| Operation | Opcode (Binary) | Opcode (Decimal) |
| LDI | 1010 | 10 |
| ADD | 0001 | 1 |
| ST | 0011 | 3 |
| JSR | 0100 | 4 |
| LEA | 1110 | 14 |

**Part C**

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction |  |  |  |
| 1100000011000000 |  |  |  |
| Opcode |  | BaseR |  |
| 1100 | 000 | 011 | 000000 |
| JMP |  | R3 |  |
| PC <- R3 |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction |  |  |  |
| 0110001100001110 |  |  |  |
| Opcode | DR | BaseR | offset6 |
| 0110 | 001 | 100 | 001110 |
| LDR | R1 | R4 | 14 |
| R1 <- content of(R4+14) |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |
| 0001001011000100 |  |  |  |  |
| Opcode | DR | SR1 |  | SR2 |
| 0001 | 001 | 011 | 000 | 100 |
| ADD | R1 | R3 |  | R4 |
| R1 <- R3 + R4 |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction |  |  |  |
| 0011101000011101 |  |  |  |
| Opcode | SR | PCoffset9 |  |
| 0011 | 101 | 000011101 |  |
| ST | R5 | 29 |  |
| Mem[29] <- R5 |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |
| 0001101010100011 |  |  |  |  |
| Opcode | DR | SR |  | Imm5 |
| 0001 | 101 | 010 | 1 | 00011 |
| ADD | R5 | R2 |  | 3 |
| R5 <- R2 + 3 |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction |  |  |  |
| 0010010000101001 |  |  |  |
| Opcode | DR | PCoffset9 |  |
| 0010 | 010 | 000101001 |  |
| LD | R2 | 41 |  |
| R2 <- content of(PC+1+41) |  |  |  |